REMARKS

Applicants respectfully request reconsideration of this application as amended. No claims have been amended. New claims 48-76 (previously claims 1-29) have been added. Claims 31-47 have been cancelled. Therefore, claims 48-76 are presented for examination.

35 U.S.C. §112 Rejection

Claims 31-47 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claims 31-47 are cancelled. Applicants submit that the rejection has been obviated by the cancellation of claims 31-47.

35 U.S.C. §102 Rejection

Claims 31-47 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lippmann et al. (Lippmann, U.S. Patent No. 4,947,410). Applicants submit that the rejection has been obviated by the cancellation of claims 31-47. Nevertheless, the present claims are patentable over Lippmann.

Lippmann discloses a nonvolatile memory with a linear array of memory cells to serially store counts by setting the cells one by one in correspondence with input pulses and when the array is full by resetting the cells one by one for successive pulses. When all of the cells are reset, a conventional binary counter is incremented and the serial count is repeated for further inputs. This procedure minimizes the erase/write sequences required to count a series of pulses. A shift register having a stage corresponding to each memory cell is used to read out the data from the linear array. Data is loaded from the array into the shift register and shifted out in a serial pulse train to a binary counter.

Applicants claim "*utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.*" Lippmann fails to disclose or suggest such a limit. Therefore, the present claims are patentable over Lippmann.

In addition, the present claims are patentable over Coppola et al (Coppola) (U.S. Patent No. 4,224,506) as recited in the Feb. 6, 2002 Office Action. Coppola discloses a volatile electronic counter wherein the count is retained over power off periods. This is accomplished by the use of a non-volatile memory with means for rapidly writing therein the contents of the volatile memory upon sensing a power down condition. Upon later sensing a power up condition, the contents of the non-volatile memory are returned to the volatile memory. Therefore, Coppola discloses a first counter based on volatile memory and a second back-up counter based on non-volatile memory with controlling updates.

Independent claim 48 recites maintaining a first value for a first counter based on a content of a volatile memory; maintaining a second value for a second counter based on a content of a non-volatile memory. As described above, Coppola discloses a volatile and non-volatile counter. However, Coppola fails to disclose that both counters are implemented to generate a monotonic count. Therefore, claim 48 is patentable over Coppola.

Claims 49-53 depend from claim 48 and include additional limitations. Therefore, claims 49-53 are also patentable over Coppola.

Independent claim 54 recites "utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value." As described above, Coppola discloses a volatile and

non-volatile counter. However, Coppola fails to disclose that both counters are implemented to generate a monotonic count. Therefore, claim 54 is patentable over Coppola.

Claim 55 depends from claim 54 and includes additional limitations. Therefore, claim 55 is also patentable over Coppola.

Independent claim 56 recites "utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value." Therefore for the reasons with respect to claim 54, claim 56 is patentable over Coppola.

Claim 57 depends from claim 56 and includes additional limitations. Therefore, claim 57 is also patentable over Coppola.

Independent claim 58 recites utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value. Therefore for the reasons with respect to claim 54, claim 58 is patentable over Coppola.

Claims 59-63 depend from claim 58 and include additional limitations. Therefore, claims 59-63 are also patentable over Coppola.

Independent claim 64 recites utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value. Therefore for the reasons with respect to claim 54, claim 64 is patentable over Coppola.

Claims 65 and 66 depend from claim 64 and include additional limitations. Therefore, claims 65 and 66 are also patentable over Coppola.

Independent claim 67 recites utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value. Therefore for the reasons with respect to claim 54, claim 67 is patentable over Coppola.

Claim 68 and 69 depend from claim 67 and include additional limitations. Therefore, claims 68 and 69 are also patentable over Coppola.

Independent claim 70 recites utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value. Therefore for the reasons with respect to claim 54, claim 70 is patentable over Coppola.

Claim 71 and 72 depend from claim 70 and include additional limitations. Therefore, claims 71 and 72 are also patentable over Coppola.

Independent claim 73 recites *utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.* Therefore for the reasons with respect to claim 54, claim 73 is patentable over Coppola.

Claim 74-76 depend from claim 73 and include additional limitations. Therefore, claims 74-76 are also patentable over Coppola.

35 U.S.C. §103 Rejection

Claims 53, 63, 66 and 69 stand rejected under 35 U.S.C. §103(a) as unpatentable over Coppola (U.S. Patent No. 4,224,506) in view of Pockrandt (U.S. Patent No. 4,768,210). Applicants submit that the present claims are patentable over Coppola even in view of Pockrandt.

Pockrandt discloses a method for the non-volatile storage of the counter including the successive storing of an actual counter reading into independent counter reading registers. Specifically, main register 8 and background register 9 are shown in Figure 1 of Pockrandt. Applicants submit that there is no suggestion or teaching in Pockrandt "*utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.*" As discussed, Coppola does not disclose or suggest such a limit. Therefore, any combination of Coppola or Pockrandt would not teach or suggest the claimed invention. Accordingly, the present claims are patentable over Coppola in view of Pockrandt.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, Applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Respectfully submitted,

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